BS170

N-Channel Enhancement Mode Field Effect Transistor

Product data sheet

1. Product profile

1.1 General description

N-Channel Enhancement Mode Field Effect Transistor in a TO-92 plastic package.

1.2 Applications

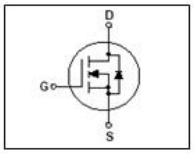
- High-speed switching applications

1.3 Quick reference data

- $V_{DSS} \geq 60$ V
- $I_D = 500$ mA
- $P_D = 0.83$ W
- $R_{DS(ON)} = 5.0$ Ω

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Symbol
1	drain D	TO-92  1. Drain 2. Gate 3. Source	
2	gate G		
3	source S		

3. Limiting values

Table 2. Limiting values

Symbol	Parameter	Conditions	Min	Unit
T_{stg}	Storage temperature		-55 — 150	℃
T_j	Junction Temperature		-55 — 150	℃
V_{DSS}	drain - source voltage		60	V
V_{GS}	Gate - source voltage		±20	V
I_D	Drain current	Tc = 25 ℃	500	mA
V_{DGR}	Drain - gate voltage(RGS≤1MΩ)		60	V
P_D	Power dissipation	Tc = 25 ℃	0.83	W

4. Characteristics

Table 3. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BVDSS	Drain - Source Breakdown Voltage	ID=100μA ,VGS=0V	60			V
IDSS	Zero gate voltage drain current	VDS =25V，VGS=0			0.5	UA
IGSS	Gate leakage current	VGS=±15V , VDS =0V			±10	nA
VGS(th)	Gate - source threshold voltage	VGS=VDS, ID =1mA	0.8		3.0	V
RDS(on)	Drain - Source on-resistance	VGS=10V, ID =200mA			5	Ω
Ciss	Input capacitance	VDS=10V, VGS=0,f=1MHz		24	40	pF
Coss	Output capacitance			17	30	pF
Crss	Reverse Transfer Capacitance			7	10	pF
td(on)	Turn-on delay time	VDS =25V,VGS=10V RL =15Ω RG= 2.5Ω （Note 2）			10	nS
td(off)	Off delay time				10	nS

* Note 1: The drain current is limited by maximum junction temperature limit.
* Note 2: Pulse Test, width ≤300μS, ≤2% duty cycle

5. Characteristic curve

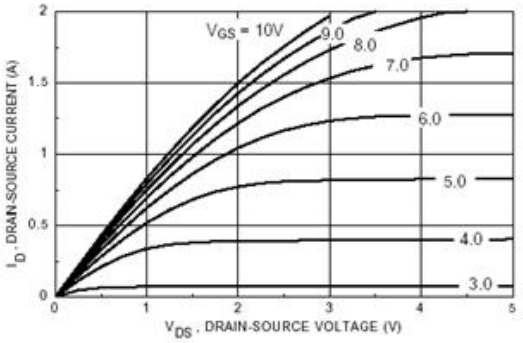


图 1 导通特性

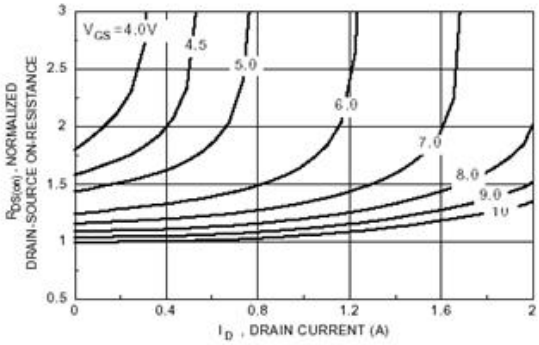


图 2 导通电阻 相对电压 漏极电流

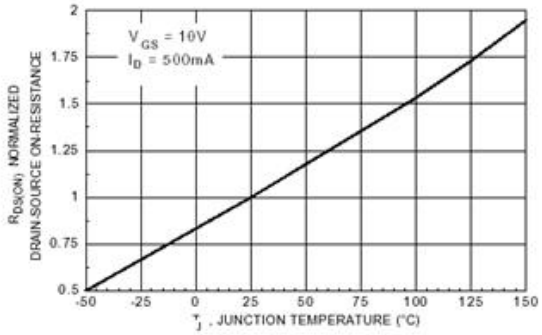


图 3 导通电阻 结温

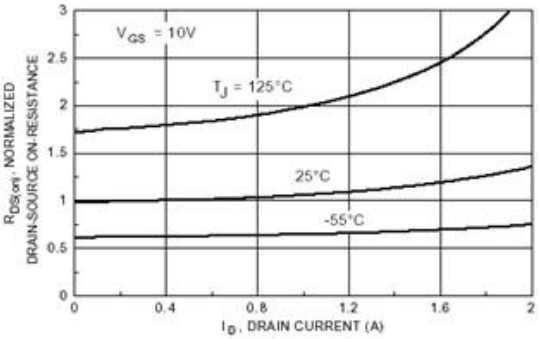


图 4 导通电阻 漏极电流 结温

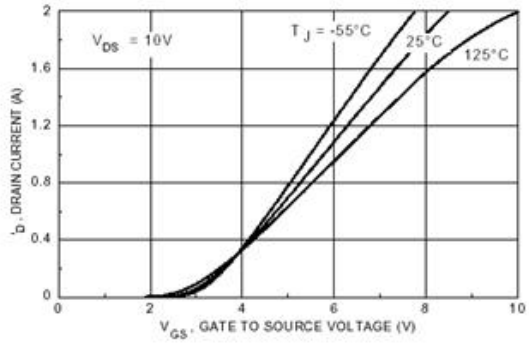


图 5 转移特性

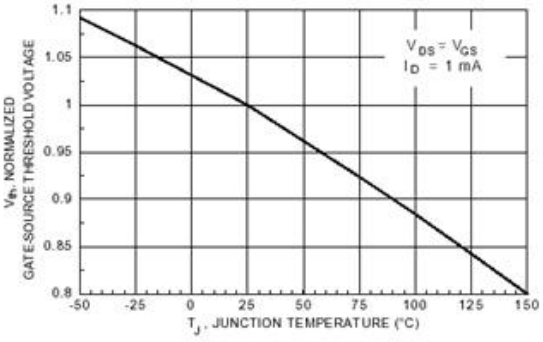


图 6 阈值开启电压 结温

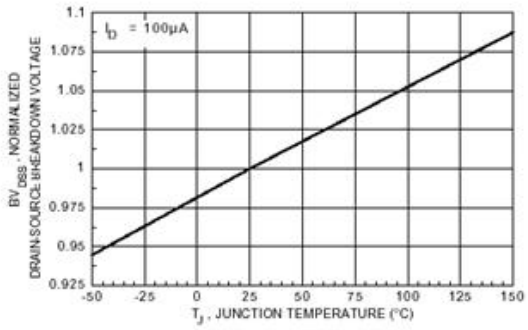


图 7 击穿电压 特性

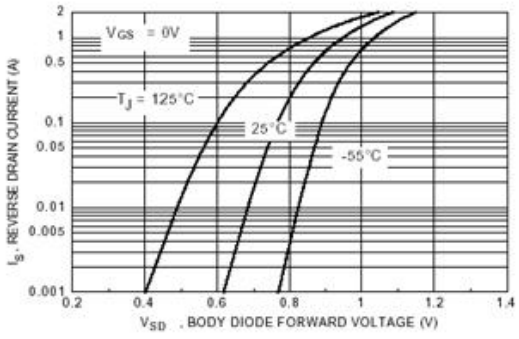


图 8 一极管正向电压 电流 特性

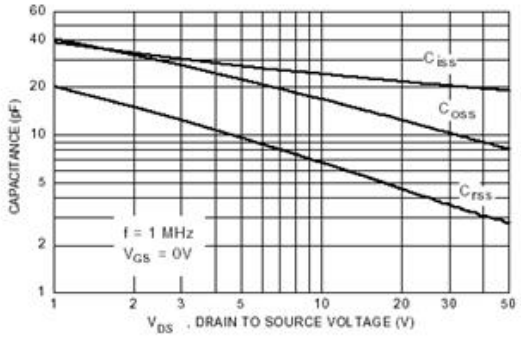


图 9 电容特性

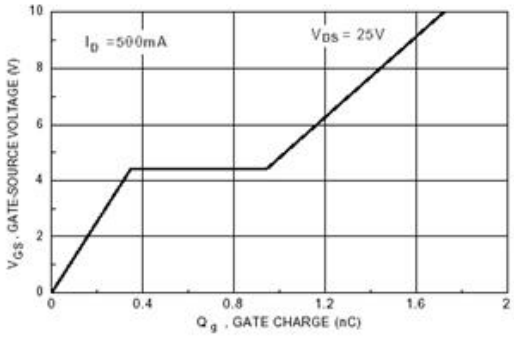


图 10 栅极电荷特性

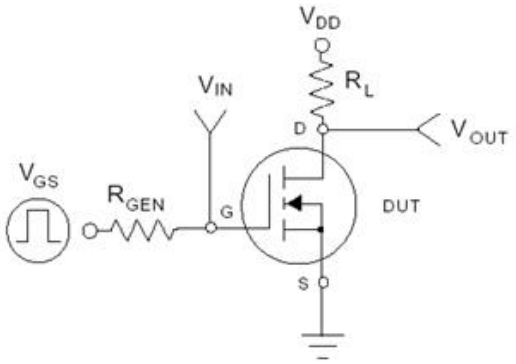


图 11 开关时间测试电路

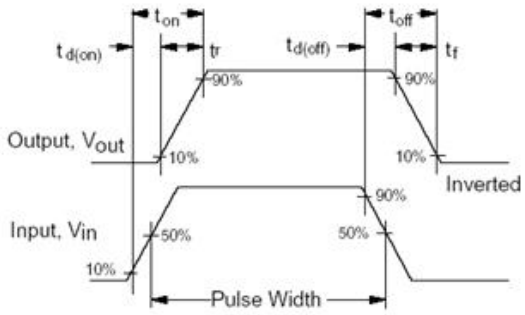


图 12 开关时间波形

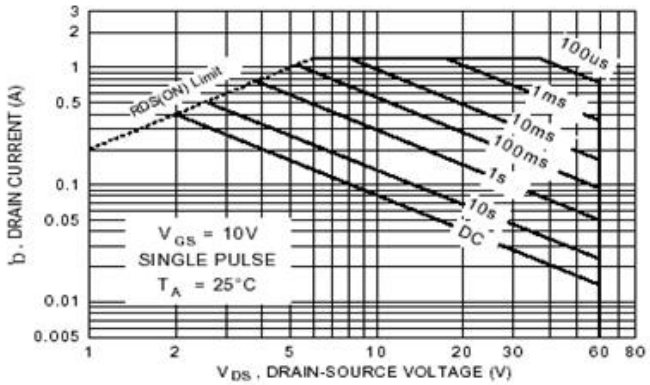


图 13 最大安全工作区

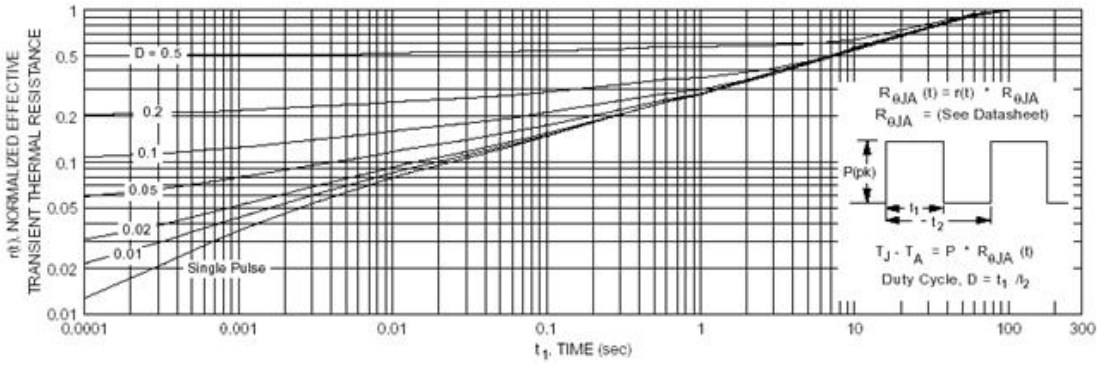


图 14 瞬态热阻