HALF-BRIDGE GATE DRIVER IC

Features

- Floating channel up to 600 V or 1200 V
- Soft over-current shutdown
- Synchronization signal to synchronize shutdown with the other phases
- Integrated desaturation detection circuit
- Two stage turn on output for di/dt control
- Separate pull-up/pull-down output drive pins
- Matched delay outputs
- Undervoltage lockout with hysteresis band
- Lead free

Description

The IR21141/IR22141 gate driver family is suited to drive a single half bridge in power switching applications. These drivers provide high gate driving capability (2 A source, 3 A sink) and require low quiescent current, which allows the use of bootstrap power supply techniques in medium power systems. These drivers feature full short circuit protection by means of power transistor desaturation detection and manage all half-bridge faults by smoothly turning off the desaturated transistor through the dedicated soft shutdown pin, therefore preventing over-voltages and reducing electromagnetic emissions. In multi-phase systems, the IR21141/IR22141 drivers communicate using a dedicated local network (SY_FLT and FAULT/SD signals) to properly manage phase-to-phase short circuits. The system controller may force shutdown or read device fault state through the 3.3 V compatible CMOS I/O pin (FAULT/SD). To improve the signal immunity from DC-bus noise, the control and power ground use dedicated pins enabling low-side emitter current sensing as well. Undervoltage conditions in floating and low voltage circuits are managed independently.

Product Summary

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOFFSET</td>
<td>600 V or 1200 V max.</td>
</tr>
<tr>
<td>IO+/− (min)</td>
<td>1.0 A / 1.5 A</td>
</tr>
<tr>
<td>VOUT</td>
<td>10.4 V – 20 V</td>
</tr>
<tr>
<td>Deadtime matching (max)</td>
<td>75 ns</td>
</tr>
<tr>
<td>Deadtime (typ)</td>
<td>330 ns</td>
</tr>
<tr>
<td>Desat blanking time (typ)</td>
<td>3 µs</td>
</tr>
<tr>
<td>DSH, DSL input voltage</td>
<td>8.0 V</td>
</tr>
<tr>
<td>Soft shutdown time (typ)</td>
<td>9.25 µs</td>
</tr>
</tbody>
</table>

Package

24-Lead SSOP

Typical connection

[Diagram of typical connection]
Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to $V_{SS}$, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_S$</td>
<td>High side offset voltage</td>
<td>$V_S - 25$</td>
<td>$V_S + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_B$</td>
<td>High side floating supply voltage</td>
<td>$V_B = 125$</td>
<td>$V_B = 625$</td>
<td></td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>High side floating output voltage (HOP, HON and SSDH)</td>
<td>$V_S - 0.3$</td>
<td>$V_S + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low side and logic fixed supply voltage</td>
<td>$-0.3$</td>
<td>$25$</td>
<td></td>
</tr>
<tr>
<td>COM</td>
<td>Power ground</td>
<td>$V_{CC} - 25$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{LO}$</td>
<td>Low side output voltage (LOP, LON and SSDL)</td>
<td>$V_{COM} - 0.3$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Logic input voltage (HIN, LIN and FLT_CLR)</td>
<td>$-0.3$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{FLT}$</td>
<td>Fault input/output voltage (FAULT/SD and SY_FLT)</td>
<td>$-0.3$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{DSH}$</td>
<td>High side DS input voltage</td>
<td>$V_S - 3$</td>
<td>$V_B + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$V_{DSL}$</td>
<td>Low side DS input voltage</td>
<td>$V_{COM} - 3$</td>
<td>$V_{CC} + 0.3$</td>
<td></td>
</tr>
<tr>
<td>$dV_s/dt$</td>
<td>Allowable offset voltage slew rate</td>
<td>—</td>
<td>$50$</td>
<td>V/ns</td>
</tr>
<tr>
<td>$P_D$</td>
<td>Package power dissipation @ $T_A \leq 25^\circ C$</td>
<td>—</td>
<td>$1.5$</td>
<td>W</td>
</tr>
<tr>
<td>$R_{thJA}$</td>
<td>Thermal resistance, junction to ambient</td>
<td>—</td>
<td>$65$</td>
<td>°C/W</td>
</tr>
<tr>
<td>$T_J$</td>
<td>Junction temperature</td>
<td>—</td>
<td>$150$</td>
<td>°C</td>
</tr>
<tr>
<td>$T_S$</td>
<td>Storage temperature</td>
<td>$-55$</td>
<td>$150$</td>
<td></td>
</tr>
<tr>
<td>$T_L$</td>
<td>Lead temperature (soldering, 10 seconds)</td>
<td>—</td>
<td>$300$</td>
<td>°C</td>
</tr>
</tbody>
</table>

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to $V_{SS}$. The $V_S$ offset rating is tested with all supplies biased at a 15 V differential.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_B$</td>
<td>High side floating supply voltage</td>
<td>$V_B = 125$</td>
<td>$V_B = 625$</td>
<td></td>
</tr>
<tr>
<td>$V_S$</td>
<td>High side floating supply offset voltage</td>
<td>$V_S = 600$</td>
<td>$V_S = 1200$</td>
<td></td>
</tr>
<tr>
<td>$V_{HO}$</td>
<td>High side output voltage (HOP, HON and SSDH)</td>
<td>$V_S$</td>
<td>$V_S + 20$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{LO}$</td>
<td>Low side output voltage (LOP, LON and SSDL)</td>
<td>$V_{COM}$</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_{CC}$</td>
<td>Low side and logic fixed supply voltage (Note 1)</td>
<td>$11.5$</td>
<td>$20$</td>
<td></td>
</tr>
<tr>
<td>COM</td>
<td>Power ground</td>
<td>$-5$</td>
<td>$5$</td>
<td></td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Logic input voltage (HIN, LIN and FLT_CLR)</td>
<td>$V_S$</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_{FLT}$</td>
<td>Fault input/output voltage (FAULT/SD and SY_FLT)</td>
<td>$V_S$</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$V_{DSH}$</td>
<td>High side DS pin input voltage</td>
<td>$V_S - 2.0$</td>
<td>$V_B$</td>
<td></td>
</tr>
<tr>
<td>$V_{DSL}$</td>
<td>Low side DS pin input voltage</td>
<td>$V_{COM} - 2.0$</td>
<td>$V_{CC}$</td>
<td></td>
</tr>
<tr>
<td>$I_{PWHIN}$</td>
<td>High side pulse width for HIN input</td>
<td>$1$</td>
<td>$\mu s$</td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Ambient temperature</td>
<td>$-40$</td>
<td>$125$</td>
<td>°C</td>
</tr>
</tbody>
</table>

† While internal circuitry is operational below the indicated supply voltages, the UV lockout disables the output drivers if the UV thresholds are not reached. A minimum supply voltage of 8V is recommended for the driver to operate safely under switching conditions at VS pin (please refer to the “start-up sequence” in application section of this document).

‡ Logic operational for $V_S$ from $V_{SS} - 5$ V to $V_{SS} + 600$ V or 1200 V. Logic state held for $V_S$ from $V_{SS} - 5$ V to $V_{SS} - V_{BS}$. For a negative spike on $V_S$ (referenced to $V_{SS}$) of less than 200ns the IC will withstand a sustained peak of -40V under normal operation and an isolated event of up to -70V peak spike (please refer to the Design Tip DT97-3 for more details).
Static Electrical Characteristics

$V_{CC} = 15 \text{ V}, V_{SS} = \text{COM} = 0 \text{ V}, V_S = 600 \text{ V or } 1200 \text{ V}$ and $T_A = 25 ^\circ \text{C}$ unless otherwise specified.

### Pins: $V_{CC}$, $V_{SS}$, $V_S$ (refer to Fig. 1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CCUV+}$</td>
<td>$V_{CC}$ supply undervoltage positive going threshold</td>
<td>9.3</td>
<td>10.2</td>
<td>11.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUV-}$</td>
<td>$V_{CC}$ supply undervoltage negative going threshold</td>
<td>8.7</td>
<td>9.3</td>
<td>10.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CCUVH}$</td>
<td>$V_{CC}$ supply undervoltage lockout hysteresis</td>
<td>—</td>
<td>0.9</td>
<td>—</td>
<td>V</td>
<td>$V_S = 0 \text{ V, } V_S = 600 \text{ V or } 1200 \text{ V}$</td>
</tr>
<tr>
<td>$V_{BSUV+}$</td>
<td>$(V_B-V_S)$ supply undervoltage positive going threshold</td>
<td>9.3</td>
<td>10.2</td>
<td>11.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{BSUV-}$</td>
<td>$(V_B-V_S)$ supply undervoltage negative going threshold</td>
<td>8.7</td>
<td>9.3</td>
<td>10.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{LK}$</td>
<td>Offset supply leakage current</td>
<td>—</td>
<td>—</td>
<td>50</td>
<td>µA</td>
<td>$V_B = V_S = 600 \text{ V or } 1200 \text{ V}$</td>
</tr>
<tr>
<td>$I_{QBS}$</td>
<td>Quiescent $V_{BS}$ supply current</td>
<td>—</td>
<td>400</td>
<td>800</td>
<td>µA</td>
<td>$V_{IN} = 0 \text{ V or } 3.3 \text{ V}$</td>
</tr>
<tr>
<td>$I_{QCC}$</td>
<td>Quiescent $V_{CC}$ supply current</td>
<td>—</td>
<td>0.7</td>
<td>2.5</td>
<td>mA</td>
<td>no load</td>
</tr>
</tbody>
</table>

### Pins: HIN, LIN, FLTCLR, FAULT/SD, SY_FLT (refer to Fig. 2, 3)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_H$</td>
<td>Logic &quot;1&quot; input voltage</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>$V_{CC} = V_{CCUV+}$ to 20 V</td>
</tr>
<tr>
<td>$V_L$</td>
<td>Logic &quot;0&quot; input voltage</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{HSS}$</td>
<td>Logic input hysteresis</td>
<td>0.2</td>
<td>0.4</td>
<td>—</td>
<td>µA</td>
<td>$V_{IN} = 3.3 \text{ V}$</td>
</tr>
<tr>
<td>$I_{H}$</td>
<td>Logic &quot;1&quot; input bias current</td>
<td>—</td>
<td>330</td>
<td>—</td>
<td>µA</td>
<td>$V_{IN} = 0 \text{ V}$</td>
</tr>
<tr>
<td>$I_{L}$</td>
<td>Logic &quot;0&quot; input bias current</td>
<td>0</td>
<td>—</td>
<td>1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$R_{ON,FLT}$</td>
<td>FAULT/SD open drain resistance</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>Ω</td>
<td>PWs 7 µs</td>
</tr>
<tr>
<td>$R_{ON,SY}$</td>
<td>SY_FLT open drain resistance</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>Ω</td>
<td></td>
</tr>
</tbody>
</table>

### Pins: DSL, DSH (refer to Fig. 4)

The active bias is present only the IR21141 and IR22141. $V_{DESAT}$, $I_{DS}$ and $I_{DSB}$ parameters are referenced to COM and $V_S$ respectively for DSL and DSH.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DESAT+}$</td>
<td>High desat input threshold voltage</td>
<td>7.2</td>
<td>8.0</td>
<td>8.8</td>
<td>V</td>
<td>See Figs. 4, 16</td>
</tr>
<tr>
<td>$V_{DESAT-}$</td>
<td>Low desat input threshold voltage</td>
<td>6.3</td>
<td>7.0</td>
<td>7.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{DS}$</td>
<td>Desat input voltage hysteresia</td>
<td>—</td>
<td>1.0</td>
<td>—</td>
<td>µA</td>
<td>$V_{DESAT} = V_{CC}$ or $V_{BS}$</td>
</tr>
<tr>
<td>$I_{DSH+}$</td>
<td>High DSH or DSL input bias current</td>
<td>—</td>
<td>21</td>
<td>—</td>
<td>µA</td>
<td>$V_{DESAT} = 0 \text{ V}$</td>
</tr>
<tr>
<td>$I_{DSH-}$</td>
<td>Low DSH or DSL input bias current</td>
<td>—</td>
<td>-160</td>
<td>—</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{DSB}$</td>
<td>DSH or DSL input bias current</td>
<td>—</td>
<td>-20</td>
<td>—</td>
<td>mA</td>
<td>$V_{DESAT} = (V_{CC} \text{ or } V_S) – 2 \text{ V}$</td>
</tr>
</tbody>
</table>
### Pins: HOP, LOP (refer to Fig. 5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>High level output voltage, $V_B - V_{HOP}$ or $V_{CC} - V_{LOP}$</td>
<td>—</td>
<td>40</td>
<td>300</td>
<td>mV</td>
<td>$I_O = 20 mA$</td>
</tr>
<tr>
<td>$I_{O1+}$</td>
<td>Output high first stage short circuit pulsed current</td>
<td>1</td>
<td>2</td>
<td>—</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$I_{O2+}$</td>
<td>Output high second stage short circuit pulsed current</td>
<td>0.5</td>
<td>1</td>
<td>—</td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>

### Pins: HON, LON, SSDH, SSDL (refer to Fig. 6)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OL}$</td>
<td>Low level output voltage, $V_{HON}$ or $V_{LON}$</td>
<td>—</td>
<td>45</td>
<td>300</td>
<td>mV</td>
<td>$I_O = 20 mA$</td>
</tr>
<tr>
<td>$R_{ON,SSD}$</td>
<td>Soft Shutdown on resistance $^\dagger$</td>
<td>—</td>
<td>90</td>
<td>—</td>
<td>Ω</td>
<td>$PW \leq 7 \mu s$</td>
</tr>
<tr>
<td>$I_O$</td>
<td>Output low short circuit pulsed current</td>
<td>1.5</td>
<td>3</td>
<td>—</td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>

$^\dagger$ SSD operation only
## AC Electrical Characteristics

$V_{CC} = V_{BS} = 15\,\text{V}$, $V_{S} = V_{SS}$ and $T_A = 25\,^\circ\text{C}$ unless otherwise specified.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{on}$</td>
<td>Turn on propagation delay</td>
<td>220</td>
<td>440</td>
<td>660</td>
<td></td>
<td>$V_{IN} = 0 &amp; 1$, $V_{S} = 0,\text{V}$ to 600,\text{V} or 1200,\text{V}, HOP shorted to HON, LOP shorted to LON, Fig. 7</td>
</tr>
<tr>
<td>$t_{off}$</td>
<td>Turn off propagation delay</td>
<td>220</td>
<td>440</td>
<td>660</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_r$</td>
<td>Turn on rise time ($C_{LOAD}=1,\text{nF}$)</td>
<td>—</td>
<td>24</td>
<td>—</td>
<td></td>
<td>$V_{HIN}=1,\text{V}$</td>
</tr>
<tr>
<td>$t_f$</td>
<td>Turn off fall time ($C_{LOAD}=1,\text{nF}$)</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td></td>
<td>$V_{DESAT}=15,\text{V}$, Fig. 10</td>
</tr>
<tr>
<td>$t_{on1}$</td>
<td>Turn on first stage duration time</td>
<td>120</td>
<td>200</td>
<td>280</td>
<td></td>
<td>$V_{DS}=15,\text{V}$, Fig. 9</td>
</tr>
<tr>
<td>$t_{DESAT1}$</td>
<td>DSH to HO soft shutdown propagation delay at HO turn on</td>
<td>2000</td>
<td>3300</td>
<td>4600</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{DESAT2}$</td>
<td>DSH to HO soft shutdown propagation delay after blanking</td>
<td>1050</td>
<td>—</td>
<td>—</td>
<td></td>
<td>$V_{DS}=15,\text{V}$, Fig. 10</td>
</tr>
<tr>
<td>$t_{DESAT3}$</td>
<td>DSL to LO soft shutdown propagation delay at LO turn on</td>
<td>2000</td>
<td>3300</td>
<td>4600</td>
<td></td>
<td>$V_{LIN}=1,\text{V}$</td>
</tr>
<tr>
<td>$t_{DESAT4}$</td>
<td>DSL to LO soft shutdown propagation delay after blanking</td>
<td>1050</td>
<td>—</td>
<td>—</td>
<td></td>
<td>$V_{DESAT}=15,\text{V}$, Fig. 10</td>
</tr>
<tr>
<td>$t_{DS}$</td>
<td>Soft shutdown minimum pulse width of desat</td>
<td>1000</td>
<td>—</td>
<td>—</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{SS}$</td>
<td>Soft shutdown duration period</td>
<td>5700</td>
<td>9250</td>
<td>13500</td>
<td></td>
<td>$V_{HIN}=1,\text{V}$</td>
</tr>
<tr>
<td>$t_{SY_FLT_DESAT1}$</td>
<td>DSH to SY_FLT propagation delay at HO turn on</td>
<td>—</td>
<td>3600</td>
<td>—</td>
<td></td>
<td>$V_{DS}=15,\text{V}$, Fig. 10</td>
</tr>
<tr>
<td>$t_{SY_FLT_DESAT2}$</td>
<td>DSH to SY_FLT propagation delay after blanking</td>
<td>1300</td>
<td>—</td>
<td>—</td>
<td></td>
<td>$V_{LIN}=1,\text{V}$</td>
</tr>
<tr>
<td>$t_{SY_FLT_DESAT3}$</td>
<td>DSL to SY_FLT propagation delay at LO turn on</td>
<td>—</td>
<td>3050</td>
<td>—</td>
<td></td>
<td>$V_{DESAT}=15,\text{V}$, Fig. 10</td>
</tr>
<tr>
<td>$t_{SY_FLT_DESAT4}$</td>
<td>DSL to SY_FLT propagation delay after blanking</td>
<td>1050</td>
<td>—</td>
<td>—</td>
<td></td>
<td>$V_{HIN}=V_{LIN}=1,\text{V}$, $V_{DESAT}=15,\text{V}$, Fig. 10</td>
</tr>
<tr>
<td>$t_{BL}$</td>
<td>DS blanking time at turn on</td>
<td>—</td>
<td>3000</td>
<td>—</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Deadtime/Delay Matching Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>DT</td>
<td>Deadtime</td>
<td>—</td>
<td>330</td>
<td>—</td>
<td></td>
<td>$V_{IN}=0,\text{V}$, $V_{DESAT}=15,\text{V}$, $V_{LIN}=1,\text{V}$, Fig. 11</td>
</tr>
<tr>
<td>MDT</td>
<td>Deadtime matching, MDT=DTH-DTL</td>
<td>—</td>
<td>—</td>
<td>75</td>
<td></td>
<td>External DT = 0 s, Fig. 11</td>
</tr>
<tr>
<td>PDM</td>
<td>Propagation delay matching, Max ($t_{on}$, $t_{off}$) – Min ($t_{on}$, $t_{off}$)</td>
<td>—</td>
<td>—</td>
<td>75</td>
<td></td>
<td>External DT &gt; 500,\text{ns}$, Fig. 7</td>
</tr>
</tbody>
</table>
**Figure 1:** Undervoltage Diagram

**Figure 2:** HIN, LIN and FLTCLR Diagram

**Figure 3:** FAULT/SD and SY_FLT Diagram

**Figure 4:** DSH and DSL Diagram

**Figure 5:** HOP and LOP Diagram

**Figure 6:** HON, LON, SSDH and SSDL Diagram
Figure 7: Switching Time Waveforms

Figure 8: Output Source Current

Figure 9: Soft Shutdown Timing Waveform
**Figure 10:** Desat Timing

**Figure 11:** Internal Deadtime Timing
Lead Assignments

24-Lead SSOP

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC} )</td>
<td>Low side gate driver supply</td>
</tr>
<tr>
<td>( V_{SS} )</td>
<td>Logic ground</td>
</tr>
<tr>
<td>HIN</td>
<td>Logic input for high side gate driver outputs (HOP/HON)</td>
</tr>
<tr>
<td>LIN</td>
<td>Logic input for low side gate driver outputs (LOP/LON)</td>
</tr>
<tr>
<td>FAULT/SD</td>
<td>Dual function (in/out) active low pin. Refer to Figs. 15, 17, and 18. As an output, indicates fault condition. As an input, shuts down the outputs of the gate driver regardless ( H_{IN}/L_{IN} ) status.</td>
</tr>
<tr>
<td>SY FLT</td>
<td>Dual function (in/out) active low pin. Refer to Figs. 15, 17, and 18. As an output, indicates SSD sequence is occurring. As an input, an active low signal freezes both output status.</td>
</tr>
<tr>
<td>FLT CLR</td>
<td>Fault clear active high input. Clears latched fault condition (see Fig. 17)</td>
</tr>
<tr>
<td>LOP</td>
<td>Low side driver sourcing output</td>
</tr>
<tr>
<td>LON</td>
<td>Low side driver sinking output</td>
</tr>
<tr>
<td>DSL</td>
<td>Low side IGBT desaturation protection input</td>
</tr>
<tr>
<td>SSDL</td>
<td>Low side soft shutdown</td>
</tr>
<tr>
<td>COM</td>
<td>Low side driver return</td>
</tr>
<tr>
<td>( V_{BS} )</td>
<td>High side gate driver floating supply</td>
</tr>
<tr>
<td>HOP</td>
<td>High side driver sourcing output</td>
</tr>
<tr>
<td>HON</td>
<td>High side driver sinking output</td>
</tr>
<tr>
<td>DSH</td>
<td>High side IGBT desaturation protection input</td>
</tr>
<tr>
<td>SSDH</td>
<td>High side soft shutdown</td>
</tr>
<tr>
<td>( V_S )</td>
<td>High side floating supply return</td>
</tr>
</tbody>
</table>
SCHMITT TRIGGER INPUT
SHOOT THROUGH PREVENTION (ST) Deadtime
INPUT HOLD LOGIC
OUTPUT SHUTDOWN LOGIC
LEVEL SHIFTER
LATCH
LOCAL DESAT PROTECTION
SOFT SHUTDOWN
UV_VBS DETECT
di/dt control
Driver
UV_VCC DETECT
LOCAL DESAT PROTECTION
SOFT SHUTDOWN
di/dt control
Driver
on/off
desat
soft shutdown
on/off
DesatHS
DesatLS
on/off (HS)
DesatHS
DesatLS
on/off (LS)
Hard ShutDown
internal Hold
SD
FAULT LOGIC management (See figure 14)

FUNCTIONAL BLOCK DIAGRAM

STATE DIAGRAM

Stable State
- FAULT
- HO=LO=0 (Normal operation)
- HO/LO=1 (Normal operation)
- UNDERVOLTAGE VCC
- SHUTDOWN (SD)
- UNDERVOLTAGE VBS
- FREEZE

Temporary State
- SOFT SHUTDOWN
- START UP SEQUENCE

System Variable
- FLT_CLR
- HIN/LIN
- UV_VCC
- UV_VBS
- DSH/L
- SY_FLT
- FAULT/SD

NOTE 1: A change of logic value of the signal labeled on lines (system variable) generates a state transition.
NOTE 2: Exiting from UNDERVOLTAGE VBS state, the HO goes high only if a rising edge event happens in HIN.
### Logic Table: Output Drivers Status Description

<table>
<thead>
<tr>
<th>INPUTS</th>
<th>INPUT/OUTPUT</th>
<th>OUTPUTS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Inputs</strong></td>
<td><strong>Output</strong></td>
<td><strong>Outputs</strong></td>
</tr>
<tr>
<td><strong>Operation</strong></td>
<td><strong>Hin</strong></td>
<td><strong>Lin</strong></td>
</tr>
<tr>
<td>Shutdown</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Fault Clear</td>
<td>H_in</td>
<td>L_in</td>
</tr>
<tr>
<td>Fault Cleared</td>
<td>H_in</td>
<td>L_in</td>
</tr>
<tr>
<td>Normal Operation</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Anti Shoot Through</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Soft Shutdown (entering)</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Soft Shutdown (finishing)</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Freeze</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Undervoltage</td>
<td>X</td>
<td>L_in</td>
</tr>
<tr>
<td></td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

† SY_FLT automatically resets after the SSD event is over, without requiring FLT_CLR to be asserted. To avoid FLT_CLR conflicting with the SSD sequence of operations, in the event of a SSD during normal operation it is recommended not to apply FLT_CLR while SY_FLT is active. At power supply start-up instead, it is recommended to keep FLT_CLR active to prevent spurious diagnostic signals being generated, as described in section 1.1 Start-Up Sequence and in section 1.4.5 Fault Management at Start-up.

†† Holding FLT_CLR high all time will not allow the gate driver to latch the FAULT status and might compromise power system protection.
1 Features Description

1.1 Start-Up Sequence

At power supply start-up, it is recommended to keep the FLT_CLR pin active until the supply voltages are properly established. This prevents spurious diagnostic signals being generated.

When the bootstrap supply topology is used for supplying the floating high side stage, the following start-up sequence is recommended (see also Fig. 12):

1. Set V_CC,
2. Set FLT_CLR pin to HIGH level,
3. Set LIN pin to HIGH level and charge the bootstrap capacitor,
4. Release LIN pin to LOW level,
5. Release FLT_CLR pin to LOW level.

![Figure 12 Start-Up Sequence](image)

A minimum 15 µs LIN and FLT-CLR pulse is required. A minimum supply voltage of 8V is recommended for the driver to operate safely under switching conditions at VS pin. At lower supply the gate driving capability decreases and might become not sufficient to counteract switching charge injected to the outputs.

1.2 Normal Operation Mode

After the start-up sequence has completed, the device becomes fully operative (see grey blocks in the State Diagram).

HIN and LIN produce driver outputs to switch accordingly, while the input logic monitors the input signals and deadtime (DT) prevent shoot-through events from occurring.

1.3 Shutdown

The system controller can asynchronously command the Hard Shutdown (HSD) through the 3.3 V compatible CMOS I/O FAULT/SD pin. This event is not latched.

In a multi-phase system, FAULT/SD signals are or-ed so the controller or one of the gate drivers can force the simultaneous shutdown of the other gate drivers through the same pin.

1.4 Fault Management

The IR21141/IR22141 is able to manage supply failure (undervoltage lockout) and transistor desaturation (on both the low and high side switches).

1.4.1 Undervoltage (UV)

The undervoltage protection function disables the driver’s output stage which prevents the power device from being driven when the input voltage is less than the undervoltage threshold. Both the low side (V_CC supplied) and the floating side (V_BS supplied) are controlled by a dedicated undervoltage function.

An undervoltage event on the V_CC pin (when \( V_{CC} < V_{CC-} \)) generates a diagnostic signal by forcing the FAULT/SD pin low (see FAULT/SD section and Fig. 14). This event disables both the low side and floating drivers and the diagnostic signal holds until the undervoltage condition is over. The fault condition is not latched and the FAULT/SD pin is released once V_CC becomes higher than UV_VCC-.

The V_BS undervoltage protection works by disabling only the floating driver. Undervoltage on V_BS does not prevent the low side driver from activating its output nor does it generate diagnostic signals. The V_BS undervoltage condition \( V_{BS} < V_{BS-} \) latches the high side output stage in the low state. V_BS must exceed the UV_VBS threshold to return the device to its normal operating mode. To turn on the floating driver, H_IN must be re-asserted high (rising edge event on H_IN is required).

1.4.2 Power Devices Desaturation

Different causes can generate a power inverter failure (phase and/or rail supply short-circuit, overload conditions induced by the load, etc.). In all of these fault conditions, a large increase in current results in the IGBT.

The IR21141/IR22141 fault detection circuit monitors the IGBT emitter to collector voltage (V_CE) (an external high voltage diode is connected between the IGBT’s collector and the ICs DSH or DSL pins). A high current in the IGBT may cause the transistor to desaturate; this condition results in an increase of V_CE.

Once in desaturation, the current in the power transistor can be as high as 10 times the nominal current. Whenever the transistor is switched off, this high current generates relevant voltage transients in the power stage that need to be smoothed out in order to avoid destruction (by over-voltage). The gate driver is able to control the transient condition by smoothly turning off the desaturated transistor with its integrated soft shutdown (SSD) protection.

1.4.3 Desaturation Detection: DSH/L Function

Figure 13 shows the structure of the desaturation sensing and soft shutdown block. This configuration is the same for both the high and low side output stages.
The external sensing diode should have breakdown voltage greater than 600 V (IR21141) or 1200 V (IR22141), and low stray capacitance (in order to minimize noise coupling and switching delays). The diode is biased by an internal pull-up resistor R_DSHEL (equal to VCE/IZS or VGS/IZS) or by a dedicated circuit (see the active-bias section). To limit the current flowing through DSH and DSL in case of desaturation an external Schottky diode is required, as shown in Fig. 13. When VCE increases, the voltage at the DSH or DSL pin increases too. Being internally biased to the local supply, the DSH/DSL voltage is automatically clamped. When DSH/DSL exceeds the V_DESAT threshold, the comparator triggers (see Fig. 13). The comparator’s output is filtered in order to avoid false desaturation detection by externally induced noise; pulses shorter than t_MIN are filtered out. To avoid detecting a false desaturation event during IGBT turn on, the desaturation circuit is disabled by a blanking signal (T_BL, see blanking block in Fig. 13). This time is the estimated maximum IGBT turn on time and must be not exceed proper gate resistance sizing. When the IGBT is not completely saturated after T_BL, desaturation is detected and the driver will turn off.

Eligible desaturation signals initiate the SSD sequence. While in SSD, the driver’s output goes to a high impedance state and the SSD pull-down is activated to turn off the IGBT through the SSDH/SSDL pin. The SY_FLT output pin (active low, see Fig. 14) reports the gate driver status during the SSD sequence (t_SD). Once the SSD has finished, SY_FLT releases, and the gate driver generates a FAULT signal (see the FAULT/SD section) by activating the FAULT/SD pin. This generates a hard shutdown for both the high and low output stages (HO=LO=low). Each driver is latched low until the fault is cleared (see FLT_CLR).

Figure 14 shows the fault management circuit. In this diagram DesatHS and DesatLS are two internal signals that come from the output stages (see Fig. 13).

It must be noted that while in SSD, both the undervoltage fault and external SD are masked until the end of SSD. Desaturation protection is working independently by the other control pin and it is disabled only when the output status is off.

1.4.4 Fault Management in Multi-Phase Systems
In a system with two or more gate drivers the IR21141/IR22141 devices must be connected as shown in Fig. 15.
Figure 15: IR22141 used in a 3 phase application

**SY_FLT:** The bi-directional SY_FLT pins communicate each other through a local network. The logic signal is active low. The device that detects the IGBT desaturation activates the SY_FLT, which is then read by the other gate drivers. When SY_FLT is active all the drivers hold their output state regardless of the input signals (HIN, LIN), they receive from the controller (freeze state). This feature is particularly important in phase-to-phase short circuit where two IGBTs are involved; in fact, while one is softly shutting-down, the other must be prevented from hard shutdown to avoid exiting SSD. In the freeze state, the frozen drivers are not completely inactive because desaturation detection still takes the highest priority. SY_FLT communication has been designed for creating a local network between the drivers.

**FAULT/SD:** The bi-directional FAULT/SD pins communicate with each other and with the system controller. The logic signal is active low. When low, the FAULT/SD signal commands the outputs to go off by hard shutdown. There are three events that can force FAULT/SD low:

1. Desaturation detection event: the FAULT/SD pin is latched low when SSD is over, and only a FLT_CLR signal can reset it.
2. Undervoltage on VCC: the FAULT/SD pin is forced low and held until the undervoltage is active. This event is not latched.
3. FAULT/SD is externally driven low either from the controller or from another IR21141/IR22141 device. This event is not latched; therefore the FLT_CLR cannot disable it. Only when FAULT/SD becomes high the device returns to its normal operating mode.

**1.4.5 Fault Management at Start-up**

When the bootstrap supply topology is used for supplying the floating high side and the recommended power supply start-up sequence is followed, FLT_CLR pin must be kept active to prevent spurious diagnostic signals being generated.

In the event of power inverter failure already present or occurring during start-up (phase and/or rail supply short-circuit, overload conditions induced by the load, etc.), keeping the FLT_CLR pin active will also prevent the real fault condition to be detected with the FAULT/SD pin. In such a condition a large current increase in the IGBT will desaturate the transistor, allowing the gate driver to detect and turn-off the desaturated transistor with the integrated soft shutdown (SSD) protection.

As with a normal SSD sequence, during SSD the SY_FLT output pin (active low, see Fig. 14) will report the gate driver status. But now, being the FLT_CLR pin already active, the gate driver will not generate a FAULT signal by activating the FAULT/SD pin and it will not enter hard shutdown.

To prevent the driver to resume charging the bootstrap capacitor, therefore re-establishing the condition that will determine again the occurrence of the large current increase in the IGBT, it is recommended to monitor the SY_FLT output pin. Should the SY_FLT output pin go low during the start-up sequence, the controller must interpret a power inverter failure is present, and stop the start-up sequence.

**1.5 Active Bias**

For the purpose of sensing the power transistor desaturation, the collector voltage is monitored (an external high voltage diode is connected between the IGBT’s collector and the IC’s DSH or DSL pin). The diode is normally biased by an internal pull up resistor connected to the local supply line (V_bw or V_cc). When the transistor is “on” the diode is conducting and the amount of current flowing in the circuit is determined by the internal pull up resistor value.

In the high side circuit, the desaturation biasing current may become relevant for dimensioning the bootstrap capacitor (see Fig. 19). In fact, a pull up resistor with a low resistance may result in a high current that significantly discharges the bootstrap capacitor. For that reason, the internal pull up resistor typical value is of the order of 100 kΩ.

While the impedance of the DSH/DSL pins is very low when the transistor is on (low impedance path through the external diode down to the power transistor), the impedance is only controlled by the pull up resistor when the transistor is off. In that case, relevant dv/dt applied by the power transistor during the commutation at the output results in a considerable current injected through the stray capacitance of the diode into the desaturation detection pin (DSH/DSL). This coupled noise may be easily reduced by using an active bias circuit for the sensing diode.

In IR21141/IR22141 the DSH/DSL pins integrate an active pull-up structure respectively to Vbw/Vcc, and a pull-down structure to Vg/COM.

The dedicated biasing circuit reduces the impedance on the DSH/DSL pin when the voltage exceeds the V_desat threshold (see Fig. 16). This low impedance helps rejecting the noise current injected by the parasitic capacitance. When the power transistor is fully on, the sensing diode is forward biased and the voltage at the DSH/DSL pin decreases. At this point the biasing circuit deactivates, to reduce the bias current of the diode as shown in Fig. 16.

In certain switching conditions (short pulses, high temperature) the recovery current of the external desaturation sensing diode might reach levels beyond the capability of the active bias circuit. In order to avoid malfunctions and damage for the IC an external Schottky
1.6 Output Stage

The structure is shown in Fig. 13 and consists of two turn on stages and one turn off stage. When the driver turns on the IGBT (see Fig. 8), a first stage is activated while an additional stage is maintained in the active state for a limited time ($t_{on1}$). This feature boosts the total driving capability in order to accommodate both a fast gate charge to the plateau voltage and dV/dt control in switching.

At turn off, a single n-channel sinks up to 3 A ($I_{O-}$) and offers a low impedance path to prevent the self-turn on due to the parasitic Miller capacitance in the power switch.

1.7 Timing and Logic State Diagrams Description

The following figures show the input/output logic diagram. Figure 17 shows the SY_FLT and FAULT/SD signals as outputs, whereas Fig. 18 shows them as inputs.

![Figure 17: I/O Timing Diagram with SY_FLT and FAULT/SD as Output](image)

![Figure 18: I/O Logic Diagram with SY_FLT and FAULT/SD as Input](image)
Referred to the timing diagram of Fig. 17:

A. When the input signals are on together the outputs go off (anti-shoot through),
B. The HO signal is on and the high side IGBT desaturates, the HO turn off softly while the SY FLT stays low. When SY FLT goes high the FAULT/SD goes low. While in SSD, if LIN goes up, LO does not change (freeze),
C. When FAULT/SD is latched low (see FAULT/SD section) FLT_CLR can disable it and the outputs go back to follow the inputs,
D. The DSH goes high but this is not read because HO is off,
E. The LO signal is on and the low side IGBT desaturates, the low side behaviour is the same as described in point B,
F. The DSL goes high but this is not read as LO is off,
G. As point A (anti-shoot through).

Referred to the timing diagram Fig. 18:

A. The device is in the hold state, regardless of input variations. The hold state results as SY FLT is forced low externally,
B. The device outputs go off by hard shutdown, externally commanded. A through B is the same sequence adopted by another IR2x14x device in SSD procedure,
C. Externally driven low FAULT/SD (shutdown state) cannot be disabled by forcing FLT_CLR (see FAULT/SD section),
D. The FAULT/SD is released and the outputs go back to follow the inputs,
E. Externally driven low FAULT/SD: outputs go off by hard shutdown (like point B),
F. As point A and B but for the low side output.
2 Sizing Tips

2.1 Bootstrap Supply

The V_{BS} voltage provides the supply to the high side driver circuitry of the gate driver. This supply sits on top of the V_S voltage and so it must be floating. The bootstrap method is used to generate the V_{BS} supply and can be used with any of the IR211(4,41)/IR221(4,41) drivers. The bootstrap supply is formed by a diode and a capacitor as connected in Fig. 19.

![Bootstrap Supply Schematic](image)

**Figure 19:** Bootstrap Supply Schematic

This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

2.2 Bootstrap Capacitor Sizing

To size the bootstrap capacitor, the first step is to establish the minimum voltage drop (\(\Delta V_{BS}\)) that we have to guarantee when the high side IGBT is on.

If \(V_{GE\text{min}}\) is the minimum gate emitter voltage we want to maintain, the voltage drop must be:

\[
\Delta V_{BS} \leq V_C - V_F - V_{GE\text{min}} - V_{CE\text{on}}
\]

under the condition,

\[
V_{GE\text{min}} > V_{BSUV}\]

where \(V_C\) is the IC voltage supply, \(V_F\) is bootstrap diode forward voltage, \(V_{GE\text{on}}\) is emitter-collector voltage of low side IGBT, and \(V_{BSUV}\) is the high-side supply undervoltage negative going threshold.

Now we must consider the influencing factors contributing V_{BS} to decrease:

- IGBT turn on required gate charge (\(Q_{G}\)),
- IGBT gate-source leakage current (\(I_{LK,GE}\)),
- Floating section quiescent current (\(I_{QBS}\)),
- Floating section leakage current (\(I_{LK}\)),
- Bootstrap diode leakage current (\(I_{LK,DIODE}\)),
- Desat diode bias when on (\(I_{DS}\)),
- Charge required by the internal level shifters (\(Q_{LS}\); typical 20 nC),
- Bootstrap capacitor leakage current (\(I_{LK,CAP}\)),
- High side on time (\(T_{HON}\)).

\(I_{LK,CAP}\) is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

Then we have:

\[
Q_{TOT} = Q_{G} + Q_{LS} + (I_{LK,GE} + I_{QBS} + I_{LK} + I_{LK,DIODE} + I_{LK,CAP} + I_{DS}) \cdot T_{HON}
\]

The minimum size of bootstrap capacitor is:

\[
C_{BOOT\text{min}} = \frac{Q_{TOT}}{\Delta V_{BS}}
\]

An example follows using IR2214SS or IR22141SS:

a) using a 25 A @ 125 °C 1200 V IGBT (IRGP30B120KD):

- \(Q_{BS} = 800 \mu A\) (datasheet IR2214);
- \(I_{LK} = 50 \mu A\) (see Static Electrical Characteristics);
- \(Q_{LS} = 20 nC\) (datasheet IRGP30B120KD);
- \(Q_{G} = 160 nC\) (datasheet IRGP30B120KD);
- \(I_{LK,GE} = 100 nA\) (reverse recovery <100 ns);
- \(I_{LK,DIODE} = 100 \mu A\)
- \(I_{LK,CAP} = 0\) (neglected for ceramic capacitor);
- \(I_{DS} = 150 \mu A\) (see Static Electrical Characteristics);
- \(T_{HON} = 100 \mu s\).

And:

- \(V_C = 15 V\)
- \(V_F = 1 V\)
- \(V_{CE\text{onmax}} = 3.1 V\)
- \(V_{GE\text{min}} = 10.5 V\)

the maximum voltage drop \(\Delta V_{BS}\) becomes

\[
\Delta V_{BS} \leq V_C - V_F - V_{GE\text{min}} - V_{CE\text{on}} = 15 V - 1 V - 10.5 V - 3.1 V = 0.4 V
\]

And the bootstrap capacitor is:

\[
C_{BOOT} \geq \frac{290 nC}{0.4 V} = 725 nF
\]

**NOTICE:** \(V_C\) has been chosen to be 15 V. Some IGBTs may require a higher supply to work correctly with the bootstrap technique. Also \(V_C\) variations must be accounted in the above formulas.

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2.3 Some Important Considerations

Voltage Ripple: There are three different cases to consider (refer to Fig. 19).

- $I_{\text{LOAD}} < 0 \, \text{A}$: the load current flows in the low side IGBT (resulting in $V_{\text{CEon}}$).
  
  $V_{BS} = V_{\text{CC}} - V_F - V_{\text{CEon}}$

  In this case we have the lowest value for $V_{BS}$. This represents the worst case for the bootstrap capacitor sizing. When the IGBT is turned off, the $V_s$ node is pushed up by the load current until the high side freewheeling diode is forward biased.

- $I_{\text{LOAD}} = 0 \, \text{A}$: the IGBT is not loaded while being on and $V_{CE}$ can be neglected
  
  $V_{BS} = V_{\text{CC}} - V_F$

- $I_{\text{LOAD}} > 0 \, \text{A}$: the load current flows through the freewheeling diode
  
  $V_{BS} = V_{\text{CC}} - V_F + V_{FP}$

  In this case we have the highest value for $V_{BS}$. Turning on the high side IGBT, $I_{\text{LOAD}}$ flows into it and $V_s$ is pulled up. To minimize the risk of undervoltage, the bootstrap capacitor should be sized according to the $I_{\text{LOAD}} < 0 \, \text{A}$ case.

Bootstrap Resistor: A resistor ($R_{\text{boot}}$) is placed in series with the bootstrap diode (see Fig. 19) in order to limit the current when the bootstrap capacitor is initially charged. We suggest not exceeding 10 $\Omega$ to avoid increasing the $V_{BS}$ time-constant. The minimum on time for charging the bootstrap capacitor or for refreshing its charge must be verified against this time-constant.

Bootstrap Capacitor: For high $t_{\text{ON}}$ designs where an electrolytic capacitor is used, its ESR must be considered. This parasitic resistance forms a voltage divider with $R_{\text{boot}}$, which generates a voltage step on $V_{BS}$ at the first charge of bootstrap capacitor. The voltage step and the related speed ($dV_{BS}/dt$) should be limited. As a general rule, ESR should meet the following constraint.

$$\frac{\text{ESR}}{\text{ESR} + R_{\text{BOOT}}} \cdot V_{\text{CC}} \leq 3 \, \text{V}$$

A parallel combination of a small ceramic capacitor and a large electrolytic capacitor is normally the best compromise, the first capacitor possesses a fast time constant and limits the $dV_{BS}/dt$ by reducing the equivalent resistance. The second capacitor provides a large capacitance to maintain the $V_{BS}$ voltage drop within the desired $\Delta V_{BS}$.

Bootstrap Diode: The diode must have a $BV > 600 \, \text{V}$ or 1200 V and a fast recovery time ($t_r < 100 \, \text{ns}$) to minimize the amount of charge fed back from the bootstrap capacitor to $V_{\text{CC}}$ supply.

2.4 Gate Resistances

The switching speed of the output transistor can be controlled by properly sizing the resistors controlling the turn-on and turn-off gate currents. The following section provides some basic rules for sizing the resistors to obtain the desired switching time and speed by introducing the equivalent output resistance of the gate driver ($R_{\text{DOn}}$ and $R_{\text{DOff}}$).

The example shown uses IGBT power transistors and Figure 20 shows the nomenclature used in the following paragraphs. In addition, $V_{ge}^*$ indicates the plateau voltage, $Q_{gc}$ and $Q_{ge}$ indicate the gate to collector and gate to emitter charge respectively.

![Figure 20: Nomenclature](image)

2.5 Sizing The Turn-On Gate Resistor

Switching-Time: For the matters of the calculation included hereafter, the switching time $t_{\text{sw}}$ is defined as the time spent to reach the end of the plateau voltage (a total $Q_{gc} + Q_{ge}$ has been provided to the IGBT gate). To obtain the desired switching time the gate resistance can be sized starting from $Q_{ge}$ and $Q_{gc}$, $V_{cc}$, $V_{ge}$ (see Fig. 21):

$$I_{\text{avg}} = \frac{Q_{gc} + Q_{ge}}{t_{\text{sw}}}$$

and

$$R_{\text{TOT}} = \frac{V_{\text{CC}} - V_{ge}^*}{I_{\text{avg}}}$$
Figure 21: \( R_{\text{Gon}} \) Sizing

where \( R_{\text{TOT}} = R_{\text{DRp}} + R_{\text{Gon}} \)

\[ R_{\text{Gon}} = \text{gate on-resistor} \]

\[ R_{\text{DRp}} = \text{driver equivalent on-resistance} \]

\[ R_{\text{DRp}} \text{ is approximately given by} \]

\[ R_{\text{DRp}} = \begin{cases} \frac{V_{\text{CC}}}{I_{o1+}} + \frac{V_{\text{CC}}}{I_{o2+}} & \text{for } t_{\text{SW}} > t_{\text{on}} \\ \frac{V_{\text{CC}}}{I_{o1+}} & \text{for } t_{\text{SW}} \leq t_{\text{on}} \end{cases} \]

(\( I_{o1+}, I_{o2+} \) and \( t_{\text{on}} \) from “Static Electrical Characteristics”).

Table 1 reports the gate resistance size for two commonly used IGBTs (calculation made using typical datasheet values and assuming \( V_{\text{CC}} = 15 \text{ V} \)).

Output Voltage Slope: The turn-on gate resistor \( R_{\text{Gon}} \) can be sized to control the output slope \((dV_{\text{out}}/dt)\). While the output voltage has a non-linear behaviour, the maximum output slope can be approximated by:

\[
\frac{dV_{\text{out}}}{dt} = \frac{I_{\text{avg}}}{C_{\text{RESoff}}} 
\]

inserting the expression yielding \( I_{\text{avg}} \) and rearranging:

\[
R_{\text{TOT}} = \frac{V_{\text{CC}} - V_{ge}^*}{C_{\text{RESoff}} \cdot \frac{dV_{\text{out}}}{dt}} 
\]

As an example, table 2 shows the sizing of gate resistance to get \( dV_{\text{out}}/dt = 5 \text{ V/ns} \) when using two popular IGBTs (typical datasheet values are used and \( V_{\text{CC}} = 15 \text{ V} \) is assumed).

NOTICE: Turn on time must be lower than \( T_{\text{BL}} \) to avoid improper desaturation detection and SSD triggering.

2.6 Sizing the Turn-Off Gate Resistor

The worst case in sizing the turn-off resistor \( R_{\text{Goff}} \) is when the collector of the IGBT in the off state is forced to commutate by an external event (e.g., the turn-on of the companion IGBT). In this case the dV/dt of the output node induces a parasitic current through \( C_{\text{RESoff}} \) flowing in \( R_{\text{Goff}} \) and \( R_{\text{DRn}} \) (see Fig. 22). If the voltage drop at the gate exceeds the threshold voltage of the IGBT, the device may self turn on, causing large oscillation and relevant cross conduction.

The transfer function between the IGBT collector and the IGBT gate then becomes:

\[
\frac{V_{ge}}{V_{\text{dc}}} = \frac{s \cdot (R_{\text{Goff}} + R_{\text{DRn}}) \cdot C_{\text{RESoff}}}{1 + s \cdot (R_{\text{Goff}} + R_{\text{DRn}}) \cdot (C_{\text{RESoff}} + C_{\text{IES}})} 
\]

which yields to a high pass filter with a pole at:

\[
1/\tau = \frac{1}{(R_{\text{Goff}} + R_{\text{DRn}}) \cdot (C_{\text{RESoff}} + C_{\text{IES}})} 
\]

As a result, when \( \tau \) is faster than the collector rise time (to be verified after calculation) the transfer function can be approximated by:

\[
\frac{V_{ge}}{V_{\text{dc}}} = \frac{s \cdot (R_{\text{Goff}} + R_{\text{DRn}}) \cdot C_{\text{RESoff}}}{1 + s \cdot (R_{\text{Goff}} + R_{\text{DRn}}) \cdot (C_{\text{RESoff}} + C_{\text{IES}})} 
\]

so that

\[
V_{th} > V_{ge} = (R_{\text{Goff}} + R_{\text{DRn}}) \cdot C_{\text{RESoff}} \cdot \frac{dV_{\text{out}}}{dt} 
\]

in the time domain. Then the condition:

\[
V_{th} > V_{ge} = (R_{\text{Goff}} + R_{\text{DRn}}) \cdot C_{\text{RESoff}} \cdot \frac{dV_{\text{out}}}{dt} 
\]

must be verified to avoid spurious turn on. Rearranging the equation yields:

\[
R_{\text{Goff}} < \frac{V_{th}}{C_{\text{RESoff}} \cdot \frac{dV_{\text{out}}}{dt} - R_{\text{DRn}}} 
\]

\( R_{\text{DRn}} \) is approximately given by
In any case, the worst condition for unwanted turn on is with very fast steps on the IGBT collector.

In that case, the collector to gate transfer function can be approximated with the capacitor divider:

\[ V_{ge} = V_{dc} \cdot \frac{C_{RESoff}}{(C_{RESoff} + C_{IES})} \]

which is driven only by IGBT characteristics.

As an example, table 3 reports \( R_{Goff} \) (calculated with the above mentioned disequation) for two popular IGBTs to withstand \( \frac{dV_{out}}{dt} = 5 \text{ V/ns} \).

**NOTICE:** The above-described equations are intended to approximate a way to size the gate resistance. A more accurate sizing may provide more precise device and PCB (parasitic) modelling.

<table>
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<tr>
<th>IGBT</th>
<th>Qge</th>
<th>Qgc</th>
<th>Vge*</th>
<th>tsw</th>
<th>Iavg</th>
<th>Rtot</th>
<th>RGon → std commercial value</th>
<th>Tsw</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRGP30B120K(D)</td>
<td>19 nC</td>
<td>82 nC</td>
<td>9 V</td>
<td>400 ns</td>
<td>0.25 A</td>
<td>24 Ω</td>
<td>RTOT - RDRp = 12.7 Ω → 10 Ω</td>
<td>→420 ns</td>
</tr>
<tr>
<td>IRG4PH30K(D)</td>
<td>10 nC</td>
<td>20 nC</td>
<td>9 V</td>
<td>200 ns</td>
<td>0.15 A</td>
<td>40 Ω</td>
<td>RTOT - RDRp = 32.5 Ω → 33 Ω</td>
<td>→202 ns</td>
</tr>
</tbody>
</table>

**Table 1: \( t_{sw} \) Driven \( R_{Gon} \) Sizing**

<table>
<thead>
<tr>
<th>IGBT</th>
<th>Qge</th>
<th>Qgc</th>
<th>Vge*</th>
<th>CRESoff</th>
<th>Rtot</th>
<th>RGon → std commercial value</th>
<th>dVout/dt</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRGP30B120K(D)</td>
<td>19 nC</td>
<td>82 nC</td>
<td>9 V</td>
<td>85 pF</td>
<td>14 Ω</td>
<td>RTOT - RDRp = 6.5 Ω → 8.2 Ω</td>
<td>→4.5 V/ns</td>
</tr>
<tr>
<td>IRG4PH30K(D)</td>
<td>10 nC</td>
<td>20 nC</td>
<td>9 V</td>
<td>14 pF</td>
<td>85 Ω</td>
<td>RTOT - RDRp = 78 Ω → 82 Ω</td>
<td>→5 V/ns</td>
</tr>
</tbody>
</table>

**Table 2: \( \frac{dV_{out}}{dt} \) Driven \( R_{Gon} \) Sizing**

<table>
<thead>
<tr>
<th>IGBT</th>
<th>Vth(min)</th>
<th>CRESoff</th>
<th>RGoff</th>
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</thead>
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<tr>
<td>IRGP30B120K(D)</td>
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<td>85 pF</td>
<td>RGoff ≤ 4 Ω</td>
</tr>
<tr>
<td>IRG4PH30K(D)</td>
<td>3</td>
<td>14 pF</td>
<td>RGoff ≤ 35 Ω</td>
</tr>
</tbody>
</table>

**Table 3: \( R_{Goff} \) Sizing**
3 PCB Layout Tips

3.1 Distance from High to Low Voltage
The IR2x14x pinout maximizes the distance between floating (from DC- to DC+) and low voltage pins. It’s strongly recommended to place components tied to floating voltage on the high voltage side of device (V_b, V_s side) while the other components are placed on the opposite side.

3.2 Ground Plane
To minimize noise coupling, the ground plane must not be placed under or near the high voltage floating side.

3.3 Gate Drive Loops
Current loops behave like antennas and are able to receive and transmit EM noise. In order to reduce the EM coupling and improve the power switch turn-on/off performances, gate drive loops must be reduced as much as possible. Figure 23 shows the high and low side gate loops.

Moreover, current can be injected inside the gate drive loop via the IGBT collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, increasing the possibility of self turn-on. For this reason, it is strongly recommended to place the three gate resistances close together and to minimize the loop area (see Fig. 23).

Figure 23: gate drive loop

3.4 Supply Capacitors
The IR2x14x output stages are able to quickly turn on an IGBT, with up to 2 A of output current. The supply capacitors must be placed as close as possible to the device pins (V_cc and V_ss for the ground tied supply, V_b and V_s for the floating supply) in order to minimize parasitic inductance/resistance.

3.5 Routing and Placement Example
Figure 24 shows one of the possible layout solutions using a 3 layer PCB. This example takes into account all the previous considerations. Placement and routing for supply capacitors and gate resistances in the high and low voltage side minimize the supply path loop and the gate drive loop. The bootstrap diode is placed under the device to have the cathode as close as possible to the bootstrap capacitor and the anode far from high voltage and close to V_cc.

Information below refers to Fig. 24:
Bootstrap section: R1, C1, D1
High side gate: R2, R3, R4
High side Desat: D2
Low side supply: C2
Low side gate: R5, R6, R7
Low side Desat: D3

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Figures 25-83 provide information on the experimental performance of the IR21141/IR22141SSPbF HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples from multiple wafer lots were tested at three temperatures (-40 °C, 25 °C, and 125 °C) in order to generate the experimental (Exp.) curve. The line labeled Exp. consist of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).
1.10  
1.50  
1.90  
2.30  
2.70

-50 -25  0  25  50  75  100  125

**Temperature (°C)**

### Figure 31. $V_{IH}$ Logic Input Voltage vs. Temperature

0.00  
0.10  
0.20  
0.30  
0.40  
0.50  
0.60

-50 -25  0  25  50  75  100  125

**Temperature (°C)**

### Figure 33. $V_{IHSS}$ HIN Logic Input Hysteresis vs. Temperature

0.70  
0.90  
1.00  
1.30  
1.60  
1.90

-50 -25  0  25  50  75  100  125

**Temperature (°C)**

### Figure 35. LIN Logic "0" Input Voltage vs. Temperature

0.10  
0.30  
0.50  
0.70  
0.90

-50 -25  0  25  50  75  100  125

**Temperature (°C)**

### Figure 36. $V_{IHSS}$ LIN Logic Input Hysteresis vs. Temperature

0.00  
0.10  
0.20  
0.30  
0.40  
0.50  
0.60  
0.70  
0.80  
0.90

-50 -25  0  25  50  75  100  125

**Temperature (°C)**

### Figure 34. LIN Logic "1" Input Voltage vs. Temperature
Figure 37. $V_{IH}$ FLTCLR Logic Input Voltage vs. Temperature

Figure 38. $V_{IL}$ FLTCLR Logic Input Voltage vs. Temperature

Figure 39. $V_{IHSS}$ FLTCLR Logic Input Hysteresis vs. Temperature

Figure 40. $V_{IL}$ SD Logic Input Voltage vs. Temperature

Figure 41. $V_{IH}$ SD Logic Input Voltage vs. Temperature

Figure 42. $V_{IHSS}$ SD Logic Input Hysteresis vs. Temperature
Figure 43. $V_{IH_{SYFLT}}$ Logic Input Voltage vs. Temperature

Figure 44. $V_{IL_{SYFLT}}$ Logic Input Voltage vs. Temperature

Figure 45. $V_{IHSS_{SYFLT}}$ Logic Input Hysteresis vs. Temperature

Figure 46. $V_{OH_{LO}}$ vs. Temperature

Figure 47. $V_{OH_{LO}}$ vs. Temperature

Figure 48. $V_{OH_{HO}}$ vs. Temperature
Figure 49. $V_{OH}$ vs. Temperature

Figure 50. $V_{DSH+}$ vs. Temperature

Figure 51. $V_{DSL+}$ vs. Temperature

Figure 52. $V_{DSH-}$ vs. Temperature

Figure 53. $V_{DSL-}$ vs. Temperature

Figure 54. FAULT/SD Open Drain Resistance vs. Temperature
Figure 55. SY_FLT Open Drain Resistance vs. Temperature

Figure 56. DTL Off Deadtime vs. Temperature

Figure 57. DTH Off Deadtime vs. Temperature

Figure 58. TonH Propagation Delay vs. Temperature

Figure 59. ToffH Propagation Delay vs. Temperature

Figure 60. TrH Turn On Rise Time vs. Temperature
Figure 61. T\text{fH} Turn Off Fall Time vs. Temperature

Figure 62. T\text{onL} Propagation Delay vs. Temperature

Figure 63. T\text{offL} Propagation Delay vs. Temperature

Figure 64. T\text{rL} Turn On Rise Time vs. Temperature

Figure 65. T\text{fL} Turn Off Fall Time vs. Temperature

Figure 66. t\text{DSAT1} vs. Temperature
Figure 67. \( t_{\text{DSAT2}} \) vs. Temperature

Figure 68. \( t_{\text{DSAT3}} \) vs. Temperature

Figure 69. \( t_{\text{DSAT4}} \) vs. Temperature

Figure 70. \( t_{\text{SSH}} \) vs. Temperature

Figure 71. \( t_{\text{SSL}} \) vs. Temperature

Figure 72. \( IO_{2+H \text{ SC Pulsed Current}} \) vs. Temperature
Figure 73. IO2+L SC Pulsed Current vs. Temperature

Figure 74. IO-H SC Pulsed Current vs. Temperature

Figure 75. IO-L SC Pulsed Current vs. Temperature

Figure 76. t\text{ONH} vs. Temperature

Figure 77. t\text{ONL} vs. Temperature

Figure 78. IO1+H SC Pulsed Current vs. Temperature
Figure 79. IO1+L SC Pulsed Current vs. Temperature

Figure 80. $I_{\text{HIN}^+}$, Logic "1" Input Bias Current vs. Temperature

Figure 81. $I_{\text{HIN}^-}$, Logic "0" Input Bias Current vs. Temperature

Figure 82. $I_{\text{LIN}^+}$, Logic "1" Input Bias Current vs. Temperature

Figure 83. $I_{\text{LIN}^-}$, Logic "0" Input Bias Current vs. Temperature
Case Outline

MINIMUM RECOMMENDED FOOTPRINT

24X 0.38 [.015]

1.78 [.070]

8.13 [.320]

4.57 [.180]

11X 0.65 [.0256]

11X 0.26924 [.0106]

NOTES

2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
5. DATUM B AND C TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM PLANE H.
7. L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDC OUTLINE MO-150AH.

24-Lead SSOP

01 8076 01

01 5537 01 MO-150AH
### Carrier Tape Dimension for 24SSOP: 2000 units per reel

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### Reel Dimensions for 24SSOP

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LEAD-FREE PART MARKING INFORMATION

ORDER INFORMATION

24-Lead SSOP IR21141SSPbF
24-Lead SSOP IR22141SSPbF

24-Lead SSOP Tape & Reel IR21141SSPbF
24-Lead SSOP Tape & Reel IR22141SSPbF